CLAIMS:

1. A packet switch having plural input sectors and output sectors, each input sector being arranged to hold at least one queue per output sector, each output sector having plural output ports and being arranged to hold at least one queue per output port wherein the input sectors are connected to the output sectors via links configured to afford speed-up of data transfer, wherein the links comprise a set of links, and wherein the switch has means for cyclically connecting different subsets of the set of links between the input sectors and the output sectors, and means responsive to statistical variations in traffic applied to input ports of said input sectors to vary the set of links.

2. A packet switch according to claim 1 wherein each input sector is arranged to hold one queue per output of the output sectors to provide virtual output queuing (VOQ).

3. A packet switch according to claim 1 wherein each input sector is arranged to hold only one queue per output sector.

4. A packet switch having plural input sectors and output sectors,

each input sector having an input sector memory and plural input ports, each port being arranged to receive packet data, the input sector memory being arranged to store plural input queues of packet data from said input ports, at least one said input queue corresponding to each respective output sector, the input sector memory having a respective output for each said input queue,

each output sector having an output sector memory and plural output ports;

the output sector memory being arranged to store plural output queues and having plural inputs for packet data and being arranged to pass packet data to a respective output port,

the packet switch further having a population of links and a control device;

wherein said population comprises plural links for carrying packet data between outputs of the input sector memory and inputs of the output sector memory, and

wherein the control device is operable to form a selection of links from said population to provide speed-up, and thereby enable packet data transfer between said outputs and inputs using said selection of links and the control device being further operable to vary said selection to cope with changing traffic conditions.

5. A packet switch as claimed in claim 4, wherein each input sector memory is arranged to store one input queue per input port of the sector for each output port of the switch.

6. A packet switch as claimed in claim 5, wherein each output sector memory is arranged to store one output queue per output port of the sector for each input port of the switch.

7. A packet switch as claimed in claim 4, wherein each input sector memory is arranged to store a single output queue per output sector for each input port of the switch.

8. A packet switch as claimed in claim 6, wherein each output sector memory is arranged to store a single output queue per output port of the sector.

9. A packet switch as claimed in any preceding claim wherein each link has a higher packet rate than the line rate of packet flow at switch input ports to provide said speed-up.

10. A packet switch as claimed in any preceding claim wherein each link has a similar packet rate to the line rate of packet flow at switch input ports.

11. A packet switch as claimed in any of claims 4-10, wherein the control device comprises a processor constructed and arranged to construct a service matrix having integer entries in units of the link rate and having row and column sums equal to said plurality such that in said units of the internal link rate, each of said integer entries exceeds the corresponding entry in a desired traffic matrix, said matrix having elements formed by the said desired offered load at the switch inputs on the basis of each input and output port; and to decompose the service matrix into its constituent permutations thereby to control said links using said permutations.

12. A method of routing packets in a packet switch having plural input sectors and output sectors, each input sector being arranged to hold at least one queue per output sector, each output sector having plural output ports and being arranged to hold at least one queue per output port the method comprising:
providing a set of links for connecting the [T J7] or each input sector queue to respective output sector queues,

connecting at least some input sector queues to respective output sector queues using a subset of said set of links, said subset affording speed-up of data transfer, and

cyclically selecting different subsets of the set of links between the input sectors and the output sectors.

13. A method according to claim 12, comprising determining statistical variations in traffic applied to input ports of said input sectors and in response thereto vary the set of links.

14. A method according to claim 13, wherein the determining step comprises monitoring input queue states.

15. A method according to claim 13, wherein the determining step comprises monitoring input packet arrivals.

16. A method according to claim 13, 14 or 15 wherein the providing step comprises constructing a service matrix having integer entries in units of the internal link rate and having row and column sums equal to said plurality such that, in said units of the internal link rate, each of said integer entries exceeds the corresponding entry in a desired traffic matrix, said desired traffic matrix having elements formed by the said desired offered load at the switch input ports on the basis of each input port and output port;

decomposing the service matrix into its constituent permutations and controlling said links using said permutations.

17 A line card interface device having plural optical paths between a first set of ports and a second set of ports, each optical path having a controllable shutter operable to enable or disable its path, the device further having means for selecting a set of said optical paths and means for cyclically connecting different subsets of the set of paths between the first and second set of ports.

18 A line card interface according to claim 17, having means responsive to statistical variations in traffic flow to the line cards for varying the set of optical paths.

19. A line card interface device for carrying traffic having a statistical distribution which varies at a given variation rate, the interface device comprising an optical selector and a control device, the optical selector having plural interface inputs for connection to a first multi-path optical connection, plural interface outputs for connection to a second multi-path optical connection, and plural optical paths connecting the interface inputs to the interface outputs, wherein the optical paths allow transfer of more packets per unit time than are incident per unit time at the plural interface inputs, thereby providing speed-up, the optical selector further having plural optical switches, each said optical switch being operable to enable passage of optical data therethrough and to prevent passage of optical data therethrough according to control signals, the speed of response to the control signals being substantially less than said line rate, and the control device having means for applying control signals to the switch control inputs at a rate corresponding to the rate of statistical variation in input traffic distribution.

20. A line card interface device according to claim 19, wherein the optical paths are spatially distinct and are greater in number than the number of the plural interface inputs to provide spatial speed-up.

21. A line card interface device according to claim 19 or 20, wherein the interface inputs and outputs are divided into input groups and output groups, each input group having a distributor, said distributor having one or more of said interface inputs and plural outputs, each output group having a multiplexer having an input, one or more interface outputs, and the optical paths comprise an optical connection wherein each input group is connectable to each output group.

22. A line card interface according to claim 21 wherein the distributor and the multiplexer are electronic.

23. A line card interface according to claim 21 wherein the distributor and the multiplexer are optical.

24. A line card interface device according to claim 21, 22 or 23 wherein each input group has a respective input group memory, said distributor having plural outputs for writing to said input group memory and each output group has a respective output group memory, said multiplexer input being connected to receive outputs from said output group memory.

25. A line card interface device according to any of claims 21-24, wherein the optical connection comprises an optical fibre device.

26. A line card interface device according to any of claims 21-25, wherein the optical connection comprises optical components providing free-space paths in use.

27. A line card interface device according to any of claims 21-26, wherein each input group has the same number of inputs as the number of outputs of said output groups.

28. A line card interface according to any of claims 21-27, wherein each memory is a dual-port memory having an input port for writing to the memory and an output port for reading from the memory.

29. A line card interface according to any of claims 2-, having latching circuitry for storing packet data for input to said interface inputs whereby said multi-path optical connections have a line rate reduced compared to said line rate.

30. A device for providing balanced packet traffic at a set of nodes, the device having a first plurality of input ports and a first plurality of output ports, packet traffic being incident at said input ports, the device comprising a first-third stages in series, the first and third stages each having said plurality of deserialisers, said plurality of multiplexers, and a fixed transpose connection, each deserialiser having at least one input and said plurality of outputs, said at least one input forming a respective one of said input ports, each multiplexer having said plurality of inputs and at least one output, said at least one output forming a respective one of said output ports, and each fixed transpose connection connecting respective outputs of each deserialiser to a respective

input of each multiplexer, and the second stage having said plurality of sets of packet data queues, each set of packet data queues comprising said plurality of queues, each set being disposed to receive data from a respective multiplexer of the first stage and to furnish data to a respective deserialiser of the third stage.

31. A method of routing packet traffic using a device having a number of input ports and said number of output ports, the method comprising:

applying packet traffic at said input ports,

deserialising signals at each input port to provide first intermediate signals, said first intermediate signals being disposed in a group of said number of signals associated with each input port, whereby said number of groups is formed;

transposing said first intermediate signals among said groups to provide transposed groups containing one first intermediate signal from each said group and multiplexing together the transposed groups of first intermediate signals, to provide said number of second intermediate signals;

distributing said second intermediate signals among said number of queue storage locations according to the output port of the second intermediate signal;

selecting data from said storage locations and serially outputting data from locations for sequential output ports;

deserialising said serially output data to provide third intermediate signals, said third intermediate signals being disposed in a group of said number of signals, whereby said number of groups is formed;

transposing said third intermediate signals among said groups to provide transposed groups containing one third intermediate signal from each said group

and multiplexing together the transposed groups of third intermediate signals, to provide said number of output signals at said output ports.

32. A method according to claim ,wherein the method includes latching packet data prior to said transposing step interface inputs whereby optical connections in said transposing steps have a line rate reduced compared to an external line rate.